

ABSTRACT OF THE DISCLOSURE

To reduce the width of isolation between the first and second p channel MIS·FETs driven by different voltages, a first p channel MIS·FET driven by a first supply voltage and a second p channel MIS·FET driven by a second supply voltage higher than the first supply voltage are arranged in the same n well of the same semiconductor substrate, and the second supply voltage is supplied as a common well bias voltage to the n well.